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Patent

Attorney's Docket No. 027260-481

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	
Michio KOMODA	Group Art Unit: 2825
Application No.: 09/921,604	Examiner: Naum B. Levin
Filed: August 6, 2001	Appeal No.:
For: CIRCUIT MODIFICATION METHOD	

BRIEF FOR APPELLANT

Mail Stop APPEAL BRIEF – PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Date: February 19, 2004

Sir:

This appeal is from the decision of the Examiner dated July 30, 2003 (Paper No. 8). Pending Claims 2-21 are reproduced in Appendix A to this brief. Appendix B contains Figures 1 and 4-6.

A check covering the $330.00 (1402) Government fee and two extra copies of this brief are being filed herewith.

The Commissioner is hereby authorized to charge any appropriate fees under 37 C.F.R. §§1.16, 1.17, and 1.21 that may be required by this paper, and to credit any overpayment, to Deposit Account No. 02-4800. A copy of this page and the signature page are submitted in triplicate.

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Table of Contents

I. Real Party in Interest

The present application is assigned to Renesas Technology Corp., who is the real party in interest.

II. Related Appeals and Interferences

There are no known currently pending related appeals or interferences in the subject application.

III. Status of Claims

Claims 2-21 remain pending in the subject application. Claim 1 was canceled in the Amendment filed January 21, 2003.

IV. Status of Amendments

A response to the final Office Action was filed on October 29, 2003. An Advisory Action was issued dated November 20, 2003. In the Advisory Action, the Examiner stated that claims 2-19 are allowed and that claims 20-21 remain rejected.

V. Summary of the Invention

When a wire 2 is located in the vicinity of another wire 1 within a semiconductor integrated circuit, as shown in Fig. 1(a), if a voltage change occurs in the wire 2, a pulsed signal wave can occur in the wire 1 because of a coupling capacity between these wires. This phenomenon is known as "glitch." (page 1, lines 10-15)

Therefore, it is necessary to determine that a glitch error occurs when the amount of glitch exceeds a certain acceptable level, and to modify the circuit so as to reduce the amount of glitch. (page 2, lines 4-7)

There is, as a prior art circuit modification method, a technique of inserting only one buffer (i.e., driver) 5 at the midpoint of the wire 1, as shown in Fig. 1(b) so as to prevent a glitch error from occurring in the wire 1. (page 2, lines 19-22)

In such a prior art circuit modification method, even if two adjacent wires have any relationship between them, since a step of inserting an additional buffer at the midpoint of a wire which is a victim is repeated until no glitch error occurs, the number of buffers to be inserted into the victim is increased. This results in an increase in either the area or power consumption of the circuit. (page 3, lines 19-25)

It is therefore an object of the present invention to provide a circuit modification method capable of preventing the number of buffers to be inserted into the circuit for the elimination of glitch errors from reaching to the over and above what is wanted. (page 4, lines 5-9)

Fig. 4(a) is a schematic circuit diagram showing a part of a semiconductor integrated circuit which is to be modified by using a circuit modification method according to a first embodiment of the present invention. It is assumed that the circuit of Fig. 4(a) is the same as the circuit of Fig. 3 in which the buffer 5 has not been inserted into the circuit yet. Drivers 3 and 4 drive wires 1 and 2 based on signals applied thereto, and set the voltages of the two wires to either a power-supply voltage or a ground voltage, respectively. Other drivers 6 and 7 receive the voltages of the wires 1 and 2, and drive wires disposed at the next stages, respectively. The wire 1 is adjacent to the other wire 2 at the next-stage side part thereof, as shown in Fig. 4(a). This circuit is the one which has already been layout-designed using a CAD (Computer Aided Design) tool. (page 13, line 21 through page 14, line 6)

In addition to the steps included in either of the above-mentioned first to fifth embodiments, a circuit modification method according to a sixth embodiment of the present invention further comprises the steps of replacing the driving circuit (driver 3) for driving the victim 1 with another driving circuit with a higher driving ability when determined that at least the aggressor 2 (or aggressor 21) causes a glitch error in the victim 1, and further determining whether the aggressor 2 (or aggressor 21) causes a glitch error in the modified victim 1. After it is determined that the aggressor 2 (or aggressor 21) causes a glitch error in the modified victim 1, the steps of determining the one or more positions where one or more buffers are to be inserted into the victim and determining the type of the one or more buffers to be

inserted, which are adopted by the above-mentioned first to fifth embodiments, can be carried out. (page 38, lines 2-18)

For example, in the case where the layout of the circuit is designed as shown in Fig. 4(a), if it is determined, in step ST2 of Fig. 5(a), that a glitch error can occur in the victim 1, the driver 3 is replaced by another driver with a higher driving ability. Concretely, a type of functional cells (a type of driver cells in this case) having the same function as the driver 3 is selected from the cell library shown in Fig. 6. If the circuit for driving the victim 1 is a NAND gate, NAND cells are selected, and if it is a NOR gate, NOR cells are selected. (page 38, lines 19-28)

And, a functional cell (driver cell in this case) having the largest driving ability (i.e., the smallest source resistance value) is further selected from among the type of functional cells selected from the cell library. The driver 3 is then replaced by the selected functional cell. (page 38, line 29 through page 39, line 4)

The amount of glitch to be caused in the victim 1, which is driven by the selected functional cell, by the aggressor 2 is calculated, and it is determined whether the calculated amount of glitch exceeds a given value Verr. When the calculated amount of glitch exceeds Verr, step ST3 of determining the one or more positions where one or more buffers are to be inserted into the victim 1 is performed, and, otherwise, no circuit modification is performed. Page 39, lines 5-12)

By improving the driving ability of the driving circuit for driving the victim 1 before determining the one or more positions where one or more buffers are to be inserted into the victim, the amount of glitch to be caused in the victim 1 in which the driving circuit has been replace by another driver cell is reduced. Therefore, there is a possibility that the number of buffers to be inserted determined in step ST3 is decreased. Furthermore, when the driving circuit for driving the victim 1 is replaced by another driver cell in accordance with the sixth embodiment, in step ST5 in Fig. 5(a), a type of buffer having a higher driving ability than that of the other driver cell and having a minimum area is selected as each of the one or more buffers to be inserted into the victim 1 from the cell library. Therefore, the selection of a type of buffer having a high driving ability can reduce the length of delay time to be caused

in the victim 1 which is otherwise increased by occurrence of glitch errors. (page 39l, line 13 through page 40, line 1)

VI. The Issue

The issue presented for review is:

A) Whether claims 20-21 were properly rejected under 35 U.S.C. §103 as being unpatentable over *Young et al* (U.S. Patent No. 6,378,109) either alone or taken with *Tam* (U.S. Patent No. 5,900,759).

VII. Grouping of Claims

Applicants respectfully submit that claims 20-21 stand or fall together as a group.

VIII. Applicant's Arguments Against the Rejection of Claims 20-21 Under 35 U.S.C. §103

A. Errors in the rejection

Applicant respectfully submits that the rejection of claims 20-21 is erroneous because the different between the claimed subject matter and the cited prior art is such that the invention would not have been obvious to a person of ordinary skill in the art at the time the invention was made. Applicant respectfully submits that the Examiner is only selecting bits and pieces from the reference without considering the remaining teachings of that reference which would lead away from the claimed invention. Furthermore, applicant respectfully submits that the Examiner is misinterpreting *Young et al* and impermissibly modifying it in light of *Tam*.

B. Limitations not described in the prior art

One limitation not described in the prior art is replacing a driving circuit for driving a predetermined wire with another one having a higher driving ability than the driving circuit.

C. Explanation of why the limitation renders the claimed subject matter unobvious over the prior art

Young et al. appears to disclose methods for designing and fabricating digital integrated circuits, and in particular to simulation and analysis of the circuit design in order to detect and eliminate excessive electric field stress on gate oxide of the transistors comprising the digital circuits. (Col. 1, lines 16-20) A method is provided for designing an integrated circuit which contains a plurality of signal lines in close proximity, such that capacitive coupling among the signal lines is operable to induce crosstalk on at least one of the signal lines. Parasitics are extracted from a trial layout of the integrated circuit, and the method further comprises the steps of: grouping the plurality of signal lines into a plurality of aggressor groups; pruning the plurality of signal lines to form a plurality of victim signal lines; building a minimum region network for each victim signal line of the plurality of victim signal lines comprising the respective victim signal line, aggressor signal lines associated with the respective victim signal line, and associated parasitics; simulating the operation of each minimum region network to determine an amount of noise induced on each respective victim signal line by the aggressor signal lines associated with the respective victim signal line, and analyzing the simulation results of each minimum region network to determine if a gate oxide integrity (GOI) violation exists. (Col. 2, line 63 through Col. 3, line 14) Selection of potential victims and their associated aggressors is a crucial step in the crosstalk verification methodology which is performed in FindVictims filtering step 711. Pruning efficiency is extremely important to reduce the crosstalk noise computation time, while not missing victims. A concept of grouping is used to perform victim/aggressor selection. A group is defined as a set of signals that could switch at the same time and hence collectively induce a glitch on a victim that is larger than if the aggressors switched at dispersed times. (Col. 9, lines 10-20) Networks having crosstalk noise violations are tabulated in step 750. In response to a detected crosstalk noise violation, the design of the IC can be modified to eliminate the violation by changing wire spacing or by insertion of repeaters in the victim signal, for example. (Col. 11, lines 57-61)

Thus, *Young et al.* merely discloses eliminating crosstalk noise by a) changing the wire spacing or b) insertion of repeaters in the victim's signal. Nothing in *Young et al.* shows, teaches or suggests replacing a driving circuit as claimed in claim 20. Applicant respectfully traverses the Examiner's statement that replacing a driving circuit with another one having the same function and a higher driving ability may be achieved by changing wire spacing or by inserting buffers/repeaters. Applicant respectfully points out that changing the wire spacing means that the spacing of the wires carrying the signals are placed further apart in order to decrease the amount of interference therebetween. This is not the same as replacing a driving circuit. Furthermore, Applicant respectfully points out that the insertion of buffers/repeaters means that additional circuits are added to the existing circuitry. Therefore, *Young et al.* teaches away from the claimed invention of replacing a circuit. Applicant respectfully submits that replacing a driving circuit means that the number of buffers to be inserted is not increased. In *Young et al.* the insertion of buffer circuits would increase the number of elements in the circuit. As described in specification of the present invention at the "Description of the Prior Art", an increase in the number of buffers to be inserted means an increase in area and power consumption of the circuit. This is the type of problem to avoid firstly. That is, *Young et al.* is technology which contains the problem to be solved by the present invention and is a starting point of the present invention. Applicants respectfully submit that changing wire spacing or inserting buffers/repeaters of *Young et al.* are completely different from replacing a driving circuit with another one having a higher driving ability as claimed in claim 20.

Tam appears to disclose a dynamic-to-static converter of a staticized flop circuit which reduces glitching in a static output thereof. (col. 1, lines 8-10) A conventional staticized flop circuit, an example of which is shown in FIGS. 1 and 2, functions to periodically evaluate a dynamic logic signal to produce a corresponding static output signal. (col. 1, lines 12-15) Glitching results at node Y when the previous value at node Y is high and the EVAL node evaluates to low. In this case, a zero-gate delay occurs in the activation of switch MC2 (driving by the clock), whereas a 1.5-gate or more delay occurs in the pull-down of node EVAL. This

increases the pull-down time of node Y prior to its being pulled back up by action of the pull-up transistor MC3. (col. 2, lines 61-67) Glitching presents problems in several respects. For example, glitching raises power consumption and requires special care when conducting electromigration studies. Moreover, glitching reduces the noise margin for the circuit receiving the flop output. In addition, the problems of glitch propagation are intensified for low-voltage applications. FIG. 3(a) illustrates the case where Vdd=1.8v, and FIG. 3(b) illustrates the case where Vdd=1.0v. It is a common practice to attempt to counter glitching by skewing the inverter of the output buffer by selecting a stronger (lower beta ratio) pull-down device MN. When Vdd=1.8v as in FIG. 3(a), the voltage drive for MN is Vgs-Vt=0.9v-0.5v=0.4v in the case of a 50% glitch in the node Y potential. By using a larger MN in the inverter, some reduction in the glitch magnitude is possible. On the other hand, at the lower supply voltage Vdd=1.0v as in FIG. 3(b), the voltage drive for MN is Vgs-Vt=0.5v-0.5v=0.0v (again in the case of a 50% glitch in the node Y potential). Thus, regardless of the size of MN, the pull-down device is cutoff and can no longer hold the node down, and the glitch therefore propagates much more easily. There have been previous attempts to overcome or reduce the effects of glitching. One approach has been to speed up the discharge rate of the EVAL node by selecting large pull-down devices with low fanout for the EVAL node. This approach, while only minimally successful, increases the device area and power usage. Other designs include selecting a high beta ratio (i.e., a stronger pull-up) for MC3 relative to that of MC1 and MC2. Still other designs employ a high fanout on node Y by increasing the size of the output buffer INVB, or (as suggested above) a weakened pull-up (i.e. a small beta ratio) of the output buffer INVB to prevent propagation of the glitch. Nevertheless, any reduction in glitch magnitude is minimal with these approaches. (col. 3, lines 1-34)

Thus, *Tam* merely discloses how to avoid a glitch in a static flop circuit. Nothing in *Tam* shows, teaches or suggests a) a glitch error caused in a predetermined wire by an aggressor comprising one or more wires or b) replacing a driving circuit for driving a predetermined wire with another driving circuit having a

higher driving ability as claimed in claim 20. Rather, *Tam* is merely directed to avoiding or minimizing glitching in a static flop circuit.

D. Why the references taken as a whole do not suggest the claimed invention and why the features disclosed in one reference may not be properly combined with features disclosed in another reference

As discussed above, *Young et al* merely discloses inserting buffer circuits into a wire which would increase the number of elements in the circuit. Nothing in *Young et al* shows, teaches or suggests replacing a driving circuit with a driving circuit having a higher driving ability as claimed in claim 20.

Tam, as discussed above, is merely directed to minimizing glitch in the static output of a staticized flop circuit. Nothing in *Tam* shows, teaches or suggests determining a glitch error caused in a predetermined wire by an aggressor comprised of one or more wires or replacing a driving circuit with a circuit having a higher driving ability as claimed in claim 20.

A combination of *Young et al* and *Tam* would not be possible since the two are directed to different inventions. In other words, nowhere in either reference is it shown, taught or suggested how reducing glitch in the static output of a staticized flop circuit such as *Tam* would be associated with insertion of buffer circuits as in *Young et al.*

Even assuming *arguendo* that *Young et al* and *Tam* could be combined, the combination would merely suggest to add additional circuits to the existing circuitry as taught by *Young et al* and that, if a staticized flop circuit is used, to control the glitch of that circuit as taught by *Tam*. Thus, nothing in the combination of *Young et al* and *Tam* shows, teaches or suggests replacing a driving circuit with another one having a higher driving ability as claimed in claim 20. Furthermore, applicant respectfully submits that nothing in the combination of *Young et al* and *Tam* would show, teach or suggest the other features as claimed in claim 21.

For all of the above stated reasons, applicant respectfully requests the Board reverses the Examiner's rejection of claims 20-21 under 35 U.S.C. §103.

IX. Conclusion

For all of the above-stated reasons, applicant respectfully requests the Honorable Board of Patent Appeals and Interferences reverses the Examiner's decision in this case, since applicant respectfully submits that the final rejection of claims 20-21 is in error. Therefore, applicant respectfully submits that claims 20-21 should be allowed.

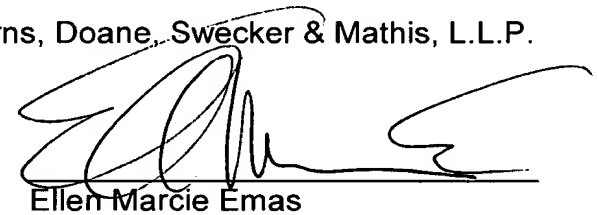
In the event that this paper is not timely filed within the currently set shortened statutory period, applicant respectfully petitions for an appropriate extension of time. The fees for such extension of time may be charged to our Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 02-4800.

Respectfully submitted,

Burns, Doane, Swecker & Mathis, L.L.P.

Date February 19, 2004

By: 

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APPENDIX A

The Appealed Claims

1. (Original) A circuit modification method of modifying a circuit by inserting one or more buffers into a predetermined wire located within the circuit, the method comprising the steps of:

determining whether a glitch error is caused in said predetermined wire by one or more aggressors each comprised of one or more other wires;

when determining that a glitch error is caused in said predetermined wire by one or more aggressors, determining one or more positions where one or more buffers are to be inserted into said predetermined wire based on a coupling capacity between each of said one or more aggressors and said predetermined wire.

2. (Previously Amended) A circuit modification method of modifying a circuit by inserting one or more buffers into a predetermined wire located within the circuit, the method comprising the steps of:

determining whether a glitch error is caused in said predetermined wire by one or more aggressors each comprised of one or more other wires;

when determining that a glitch error is caused in said predetermined wire by one or more aggressors, determining one or more positions where one or more buffers are to be inserted into said predetermined wire based on a coupling capacity between each of said one or more aggressors and said predetermined wire, wherein said insertion position determining step includes the steps of, when determining that a glitch error is caused in said predetermined wire by only one aggressor, calculating a target coupling capacity using the coupling capacity between said aggressor and said predetermined wire, and, when dividing said predetermined wire into a plurality of wire segments, determining one or more internal points of division of said predetermined wire so that a coupling capacity between each of said plurality of wire

segments and said aggressor does not exceed said target coupling capacity, and setting said one or more internal points of division to said one or more positions where said one or more buffers are to be inserted into said predetermined wire.

3. (Original) The circuit modification method according to Claim 2, wherein said target coupling capacity calculating step is the step of calculating said target coupling capacity by using an amount of glitch to be caused in said predetermined wire by said aggressor.

4. (Original) The circuit modification method according to Claim 3, wherein said target coupling capacity calculating step includes the steps of determining the number of said plurality of wire segments based on said amount of glitch, and calculating said target coupling capacity based on said coupling capacity between said aggressor and said predetermined wire and the number of said plurality determined in the above step.

5. (Original) The circuit modification method according to Claim 4, wherein said wire segment number determining step is the step of, when the coupling capacity between said aggressor and said predetermined wire is Cc, said amount of glitch is V, and a predetermined value is Vmax, determining the smallest integer number n which satisfies a following relationship: $V/n \leq Vmax$ as the number of said plurality of wire segments, and wherein said target coupling capacity calculating step is the step of calculating said target coupling capacity as follows: Cc/n, and said internal division point determining step is the step of determining said one or more internal points of division so that the coupling capacity between each of said plurality of wire segment and said aggressor is equal to said target coupling capacity Cc/n.

6. (Original) The circuit modification method according to Claim 3, wherein said target coupling capacity calculating step is the step of, when the coupling capacity between said aggressor and said predetermined wire is Cc, said amount of glitch is V, and a predetermined value is Vmax, calculating said target coupling capacity as follows: Cc*Vmax/V.

7. (Previously Amended) The circuit modification method according to Claim 2, wherein said one or more buffers to be inserted into said predetermined wire have a driving ability equal to or greater than that of a driving circuit for driving said predetermined wire.

8. (Original) The circuit modification method according to Claim 7, further comprising the step of selecting a type of buffer having a driving ability equal to or greater than that of said driving circuit for driving said predetermined wire and having a minimum area as each of said one or more buffers to be inserted into said predetermined wire from among a plurality of buffer cells stored in a cell library.

9. (Previously Amended) The circuit modification method according to Claim 2, further comprising the steps of, when determining that a glitch error is caused in said predetermined wire by one or more aggressors, replacing a driving circuit for driving said predetermined wire with another one having a higher driving ability than the driving circuit, and, before performing said insertion position determining step, determining whether a glitch error is caused in said predetermined wire driven by the other driving circuit by said one or more aggressors.

10. (Previously Amended) A circuit modification method of modifying a circuit by inserting one or more buffers into a predetermined wire located within the circuit, the method comprising the steps of:

determining whether a glitch error is caused in said predetermined wire by one or more aggressors each comprised of one or more other wires;

when determining that a glitch error is caused in said predetermined wire by one or more aggressors, determining one or more positions where one or more buffers are to be inserted into said predetermined wire based on a coupling capacity between each of said one or more aggressors and said predetermined wire, wherein said insertion position determining step includes the steps of, when determining that a glitch error is caused in said predetermined wire by a plurality of aggressors, calculating a plurality of target coupling capacities respectively associated with said plurality of aggressors by using the coupling capacity between each of said plurality of aggressors and said predetermined wire, and, when diving said predetermined wire into a plurality of wire segments, determining one or more internal points of division of said predetermined wire so that a coupling capacity between each of said plurality of wire segments and each of said plurality of aggressors does not exceed a corresponding one of said plurality of target coupling capacities, and setting said one or more internal points of division to said one or more positions where said one or more buffers are to be inserted into said predetermined wire.

11. (Original) The circuit modification method according to Claim 10, wherein said target coupling capacity calculating step includes the steps of, when the coupling capacity between each of said plurality of aggressors (referred to as *ith* (i=1 to k, k is the number of aggressors) aggressor hereafter) and said predetermined wire is Cc_i (i=1 to k), an amount of glitch to be caused in said predetermined wire by the *ith* aggressor is V_i (i=1 to k), and a predetermined value is Vmax, determining the smallest integer number n_i (i=1 to k) which satisfies a following relationship: $V_i/n_i \leq Vmax$ (i=1 to k) as the number of said plurality of wire segments for each of said plurality of aggressors, and calculating each of said plurality of target coupling capacities as follows: Cc_i/n_i (i=1 to k).

12. (Original) The circuit modification method according to Claim 10, wherein said insertion position determining step includes the steps of when dividing said predetermined wire into a plurality of wire segments for each of said plurality of aggressors, determining said one or more internal points of division of said predetermined wire so that the coupling capacity between each of said plurality of wire segment and each of said plurality of aggressor is equal to said corresponding target coupling capacity, and selecting said one or more positions where one or more buffers to be inserted into said predetermined wire from among all internal points of division determined in the above step for said plurality of aggressors.

13. (Original) The circuit modification method according to Claim 11, wherein said insertion position determining step includes the steps of when dividing said predetermined wire into a plurality of wire segments for each of said plurality of aggressors, i.e., said *ith* aggressor, determining said one or more internal points of division of said predetermined wire so that the coupling capacity between each of said plurality of wire segment and said *ith* aggressor is equal to said corresponding target coupling capacity Cc_i/n_i (i=1 to k), and selecting said one or more positions where one or more buffers to be inserted into said predetermined wire from among all internal points of division determined in the above step for said plurality of aggressors.

14. (Original) The circuit modification method according to Claim 10, wherein said target coupling capacity calculating step includes the steps of, when the coupling capacity between each of said plurality of aggressors (referred to as *ith* (i=1 to k, k is the number of aggressors) aggressor hereafter) and said predetermined wire is Cc_i (i=1 to k), an amount of glitch to be caused in said predetermined wire by said *ith* aggressor is V_i (i=1 to k), and a predetermined value is Vmax, calculating each of said plurality of target coupling capacities as follows: Cc_i*Vmax/V_i (i=1 to k).

15. (Original) A circuit modification method of modifying a circuit by inserting one or more buffers into a predetermined wire located within the circuit, the method comprising the steps of:

determining whether a glitch error is caused in said predetermined wire by an aggressor comprised of one or more other wires;

when determining that a glitch error is caused in said predetermined wire by an aggressor, determining a number of buffers to be inserted into said predetermined wire based on an amount of glitch to be caused in said predetermined wire by said aggressor.

16. (Original) The circuit modification method according to Claim 15, wherein said buffer number determining step is the step of, when said amount of glitch is V and a predetermined value is Vmax, calculating the smallest integer number n which satisfies a following relationship: $V/n \leq Vmax$.

17. (Original) The circuit modification method according to Claim 15, wherein said one or more buffers to be inserted into said predetermined wire have a

driving ability equal to or greater than that of a driving circuit for driving said predetermined wire.

18. (Original) The circuit modification method according to Claim 17, further comprising the step of selecting a type of buffer having a driving ability equal to or greater than that of said driving circuit for driving said predetermined wire and having a minimum area as each of said one or more buffers to be inserted into said predetermined wire from among a plurality of buffer cells stored in a cell library.

19. (Original) The circuit modification method according to Claim 15, further comprising the steps of, when determining that a glitch error is caused in said predetermined wire by one aggressor, replacing a driving circuit for driving said predetermined wire with another one having a higher driving ability than the driving circuit, and, before performing said buffer number determining step, determining whether a glitch error is caused in said predetermined wire driven by the other driving circuit by said one aggressor.

20. (Original) A circuit modification method comprising the steps of:

determining whether a glitch error is caused in said predetermined wire by an aggressor comprised of one or more other wires;

when determining that a glitch error is caused in said predetermined wire by an aggressor, replacing a driving circuit for driving said predetermined wire with another one having a higher driving ability than the driving circuit.

21. (Previously Presented) The circuit modification method according to claim 20, wherein said another driving circuit has a same function as the driving circuit.

APPENDIX B

Figures 1 and 4-6

APPENDIX B

Figures 1 and 4-6

FIG.1(a)

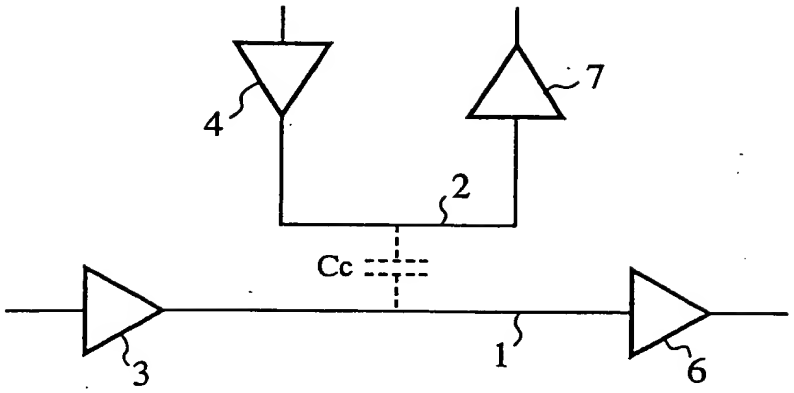


FIG.1(b)
(PRIOR ART)

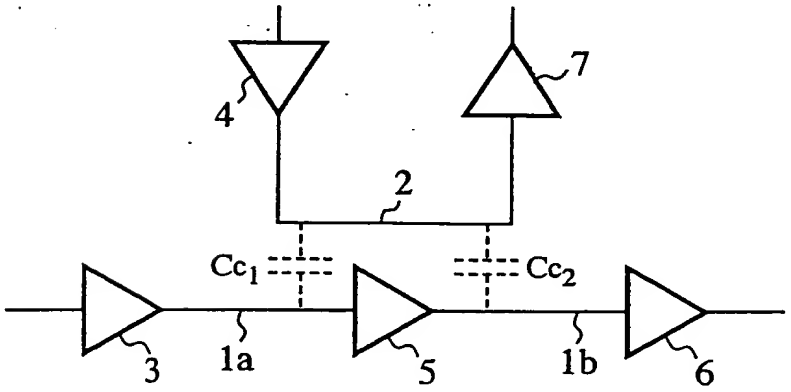


FIG.4(a)

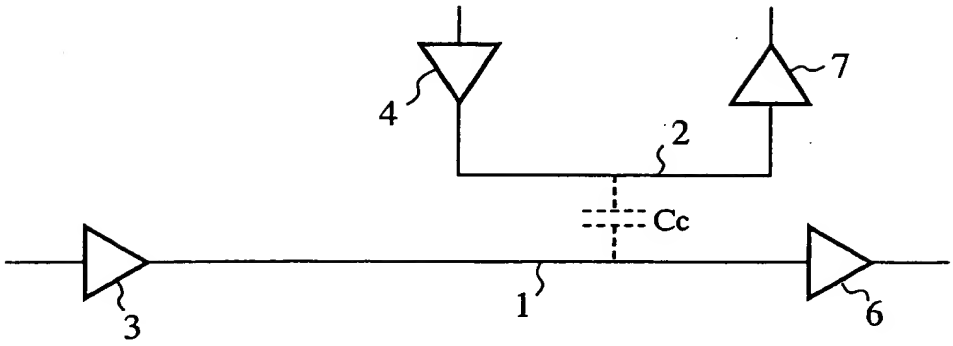


FIG.4(b)

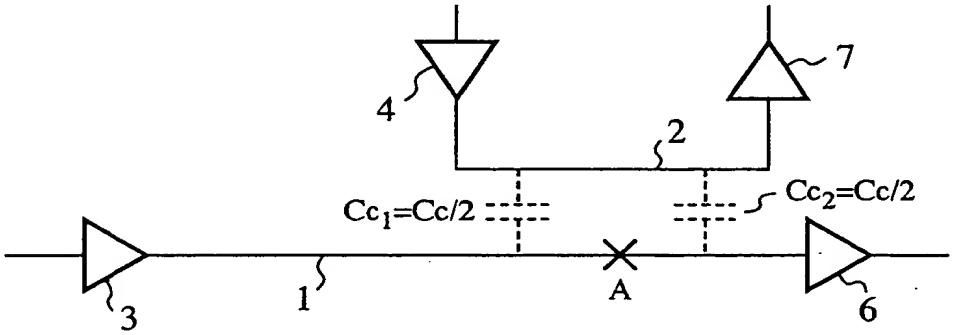


FIG.4(c)

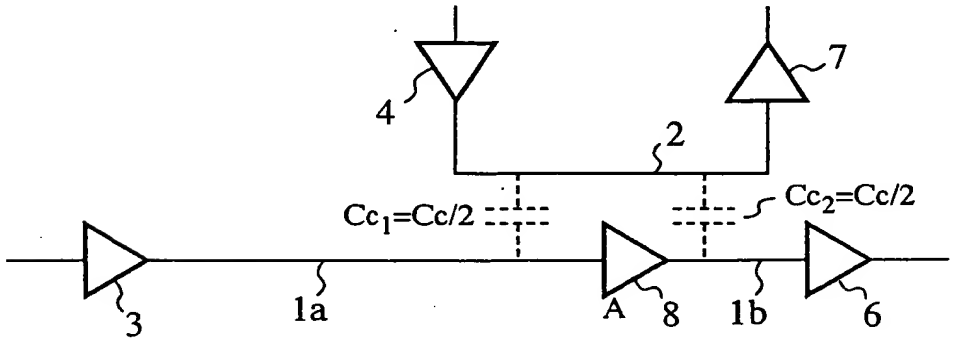


FIG.5(a)

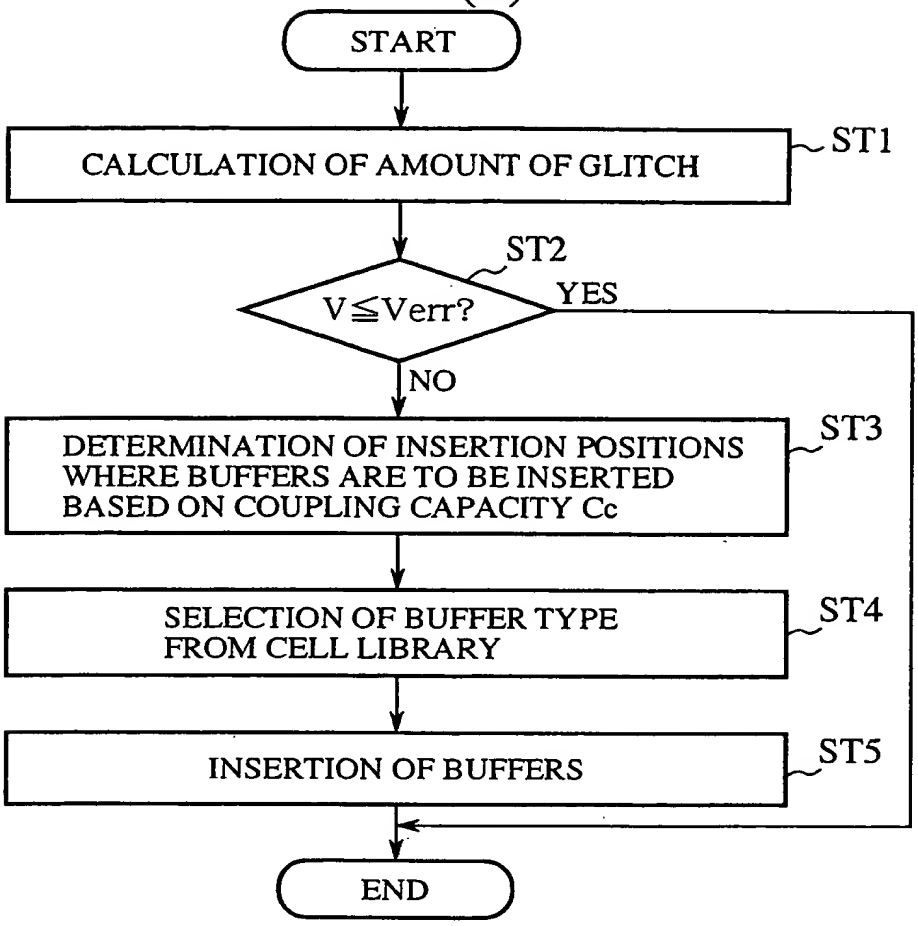


FIG.5(b)

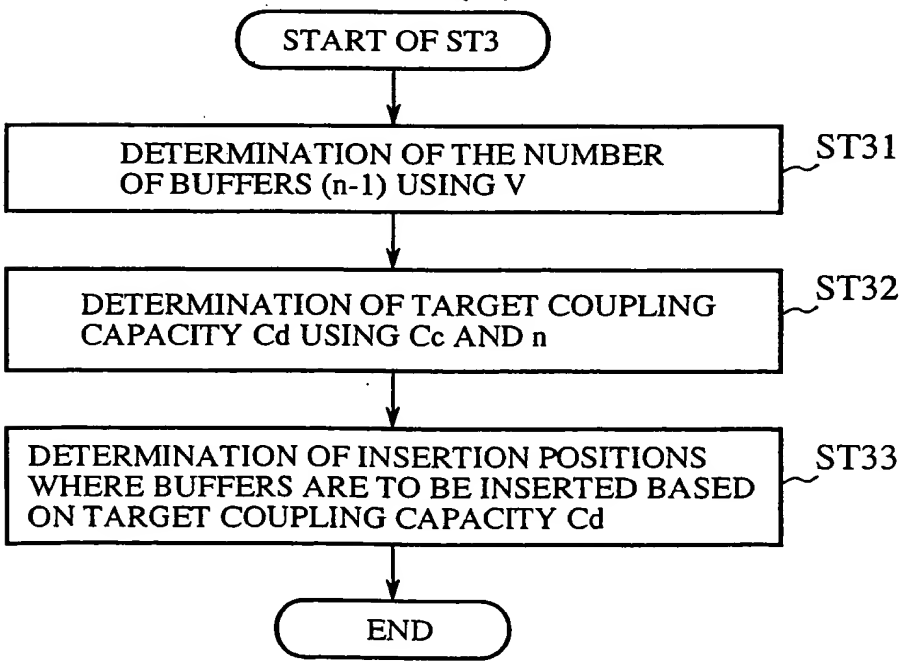


FIG.6

CELL TYPE	PARAMETERS			
	AREA	DRIVING ABILITY	. . .	. . .
INVERTER 1	X1(μm^2)	Y1(Ω)		
INVERTER 2	X2(μm^2)	Y2(Ω)		
DRIVER 1	X3(μm^2)	Y3(Ω)		
DRIVER 2	X4(μm^2)	Y4(Ω)		
NAND1	X5(μm^2)	Y5(Ω)		
NAND2	X6(μm^2)	Y6(Ω)		

Patent
Attorney's Docket No. 027260-481

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	
Michio KOMODA	Group Art Unit: 2825
Application No.: 09/921,604	Examiner: Naum B. Levin
Filed: August 6, 2001	Appeal No.:
For: CIRCUIT MODIFICATION METHOD	

BRIEF FOR APPELLANT

Mail Stop APPEAL BRIEF – PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Date: February 19, 2004

Sir:

This appeal is from the decision of the Examiner dated July 30, 2003 (Paper No. 8). Pending Claims 2-21 are reproduced in Appendix A to this brief. Appendix B contains Figures 1 and 4-6.

A check covering the $330.00 (1402) Government fee and two extra copies of this brief are being filed herewith.

The Commissioner is hereby authorized to charge any appropriate fees under 37 C.F.R. §§1.16, 1.17, and 1.21 that may be required by this paper, and to credit any overpayment, to Deposit Account No. 02-4800. A copy of this page and the signature page are submitted in triplicate.

Table of Contents

I. Real Party in Interest

The present application is assigned to Renesas Technology Corp., who is the real party in interest.

II. Related Appeals and Interferences

There are no known currently pending related appeals or interferences in the subject application.

III. Status of Claims

Claims 2-21 remain pending in the subject application. Claim 1 was canceled in the Amendment filed January 21, 2003.

IV. Status of Amendments

A response to the final Office Action was filed on October 29, 2003. An Advisory Action was issued dated November 20, 2003. In the Advisory Action, the Examiner stated that claims 2-19 are allowed and that claims 20-21 remain rejected.

V. Summary of the Invention

When a wire 2 is located in the vicinity of another wire 1 within a semiconductor integrated circuit, as shown in Fig. 1(a), if a voltage change occurs in the wire 2, a pulsed signal wave can occur in the wire 1 because of a coupling capacity between these wires. This phenomenon is known as "glitch." (page 1, lines 10-15)

Therefore, it is necessary to determine that a glitch error occurs when the amount of glitch exceeds a certain acceptable level, and to modify the circuit so as to reduce the amount of glitch. (page 2, lines 4-7)

There is, as a prior art circuit modification method, a technique of inserting only one buffer (i.e., driver) 5 at the midpoint of the wire 1, as shown in Fig. 1(b) so as to prevent a glitch error from occurring in the wire 1. (page 2, lines 19-22)

In such a prior art circuit modification method, even if two adjacent wires have any relationship between them, since a step of inserting an additional buffer at the midpoint of a wire which is a victim is repeated until no glitch error occurs, the number of buffers to be inserted into the victim is increased. This results in an increase in either the area or power consumption of the circuit. (page 3, lines 19-25)

It is therefore an object of the present invention to provide a circuit modification method capable of preventing the number of buffers to be inserted into the circuit for the elimination of glitch errors from reaching to the over and above what is wanted. (page 4, lines 5-9)

Fig. 4(a) is a schematic circuit diagram showing a part of a semiconductor integrated circuit which is to be modified by using a circuit modification method according to a first embodiment of the present invention. It is assumed that the circuit of Fig. 4(a) is the same as the circuit of Fig. 3 in which the buffer 5 has not been inserted into the circuit yet. Drivers 3 and 4 drive wires 1 and 2 based on signals applied thereto, and set the voltages of the two wires to either a power-supply voltage or a ground voltage, respectively. Other drivers 6 and 7 receive the voltages of the wires 1 and 2, and drive wires disposed at the next stages, respectively. The wire 1 is adjacent to the other wire 2 at the next-stage side part thereof, as shown in Fig. 4(a). This circuit is the one which has already been layout-designed using a CAD (Computer Aided Design) tool. (page 13, line 21 through page 14, line 6)

In addition to the steps included in either of the above-mentioned first to fifth embodiments, a circuit modification method according to a sixth embodiment of the present invention further comprises the steps of replacing the driving circuit (driver 3) for driving the victim 1 with another driving circuit with a higher driving ability when determined that at least the aggressor 2 (or aggressor 21) causes a glitch error in the victim 1, and further determining whether the aggressor 2 (or aggressor 21) causes a glitch error in the modified victim 1. After it is determined that the aggressor 2 (or aggressor 21) causes a glitch error in the modified victim 1, the steps of determining the one or more positions where one or more buffers are to be inserted into the victim and determining the type of the one or more buffers to be

inserted, which are adopted by the above-mentioned first to fifth embodiments, can be carried out. (page 38, lines 2-18)

For example, in the case where the layout of the circuit is designed as shown in Fig. 4(a), if it is determined, in step ST2 of Fig. 5(a), that a glitch error can occur in the victim 1, the driver 3 is replaced by another driver with a higher driving ability. Concretely, a type of functional cells (a type of driver cells in this case) having the same function as the driver 3 is selected from the cell library shown in Fig. 6. If the circuit for driving the victim 1 is a NAND gate, NAND cells are selected, and if it is a NOR gate, NOR cells are selected. (page 38, lines 19-28)

And, a functional cell (driver cell in this case) having the largest driving ability (i.e., the smallest source resistance value) is further selected from among the type of functional cells selected from the cell library. The driver 3 is then replaced by the selected functional cell. (page 38, line 29 through page 39, line 4)

The amount of glitch to be caused in the victim 1, which is driven by the selected functional cell, by the aggressor 2 is calculated, and it is determined whether the calculated amount of glitch exceeds a given value Verr. When the calculated amount of glitch exceeds Verr, step ST3 of determining the one or more positions where one or more buffers are to be inserted into the victim 1 is performed, and, otherwise, no circuit modification is performed. Page 39, lines 5-12)

By improving the driving ability of the driving circuit for driving the victim 1 before determining the one or more positions where one or more buffers are to be inserted into the victim, the amount of glitch to be caused in the victim 1 in which the driving circuit has been replace by another driver cell is reduced. Therefore, there is a possibility that the number of buffers to be inserted determined in step ST3 is decreased. Furthermore, when the driving circuit for driving the victim 1 is replaced by another driver cell in accordance with the sixth embodiment, in step ST5 in Fig. 5(a), a type of buffer having a higher driving ability than that of the other driver cell and having a minimum area is selected as each of the one or more buffers to be inserted into the victim 1 from the cell library. Therefore, the selection of a type of buffer having a high driving ability can reduce the length of delay time to be caused

in the victim 1 which is otherwise increased by occurrence of glitch errors. (page 39l, line 13 through page 40, line 1)

VI. The Issue

The issue presented for review is:

A) Whether claims 20-21 were properly rejected under 35 U.S.C. §103 as being unpatentable over *Young et al* (U.S. Patent No. 6,378,109) either alone or taken with *Tam* (U.S. Patent No. 5,900,759).

VII. Grouping of Claims

Applicants respectfully submit that claims 20-21 stand or fall together as a group.

VIII. Applicant's Arguments Against the Rejection of Claims 20-21 Under 35 U.S.C. §103

A. Errors in the rejection

Applicant respectfully submits that the rejection of claims 20-21 is erroneous because the different between the claimed subject matter and the cited prior art is such that the invention would not have been obvious to a person of ordinary skill in the art at the time the invention was made. Applicant respectfully submits that the Examiner is only selecting bits and pieces from the reference without considering the remaining teachings of that reference which would lead away from the claimed invention. Furthermore, applicant respectfully submits that the Examiner is misinterpreting *Young et al* and impermissibly modifying it in light of *Tam*.

B. Limitations not described in the prior art

One limitation not described in the prior art is replacing a driving circuit for driving a predetermined wire with another one having a higher driving ability than the driving circuit.

C. Explanation of why the limitation renders the claimed subject matter unobvious over the prior art

Young et al. appears to disclose methods for designing and fabricating digital integrated circuits, and in particular to simulation and analysis of the circuit design in order to detect and eliminate excessive electric field stress on gate oxide of the transistors comprising the digital circuits. (Col. 1, lines 16-20) A method is provided for designing an integrated circuit which contains a plurality of signal lines in close proximity, such that capacitive coupling among the signal lines is operable to induce crosstalk on at least one of the signal lines. Parasitics are extracted from a trial layout of the integrated circuit, and the method further comprises the steps of: grouping the plurality of signal lines into a plurality of aggressor groups; pruning the plurality of signal lines to form a plurality of victim signal lines; building a minimum region network for each victim signal line of the plurality of victim signal lines comprising the respective victim signal line, aggressor signal lines associated with the respective victim signal line, and associated parasitics; simulating the operation of each minimum region network to determine an amount of noise induced on each respective victim signal line by the aggressor signal lines associated with the respective victim signal line, and analyzing the simulation results of each minimum region network to determine if a gate oxide integrity (GOI) violation exists. (Col. 2, line 63 through Col. 3, line 14) Selection of potential victims and their associated aggressors is a crucial step in the crosstalk verification methodology which is performed in FindVictims filtering step 711. Pruning efficiency is extremely important to reduce the crosstalk noise computation time, while not missing victims. A concept of grouping is used to perform victim/aggressor selection. A group is defined as a set of signals that could switch at the same time and hence collectively induce a glitch on a victim that is larger than if the aggressors switched at dispersed times. (Col. 9, lines 10-20) Networks having crosstalk noise violations are tabulated in step 750. In response to a detected crosstalk noise violation, the design of the IC can be modified to eliminate the violation by changing wire spacing or by insertion of repeaters in the victim signal, for example. (Col. 11, lines 57-61)

Thus, *Young et al.* merely discloses eliminating crosstalk noise by a) changing the wire spacing or b) insertion of repeaters in the victim's signal. Nothing in *Young et al.* shows, teaches or suggests replacing a driving circuit as claimed in claim 20. Applicant respectfully traverses the Examiner's statement that replacing a driving circuit with another one having the same function and a higher driving ability may be achieved by changing wire spacing or by inserting buffers/repeaters. Applicant respectfully points out that changing the wire spacing means that the spacing of the wires carrying the signals are placed further apart in order to decrease the amount of interference therebetween. This is not the same as replacing a driving circuit. Furthermore, Applicant respectfully points out that the insertion of buffers/repeaters means that additional circuits are added to the existing circuitry. Therefore, *Young et al.* teaches away from the claimed invention of replacing a circuit. Applicant respectfully submits that replacing a driving circuit means that the number of buffers to be inserted is not increased. In *Young et al.* the insertion of buffer circuits would increase the number of elements in the circuit. As described in specification of the present invention at the "Description of the Prior Art", an increase in the number of buffers to be inserted means an increase in area and power consumption of the circuit. This is the type of problem to avoid firstly. That is, *Young et al.* is technology which contains the problem to be solved by the present invention and is a starting point of the present invention. Applicants respectfully submit that changing wire spacing or inserting buffers/repeaters of *Young et al.* are completely different from replacing a driving circuit with another one having a higher driving ability as claimed in claim 20.

Tam appears to disclose a dynamic-to-static converter of a staticized flop circuit which reduces glitching in a static output thereof. (col. 1, lines 8-10) A conventional staticized flop circuit, an example of which is shown in FIGS. 1 and 2, functions to periodically evaluate a dynamic logic signal to produce a corresponding static output signal. (col. 1, lines 12-15) Glitching results at node Y when the previous value at node Y is high and the EVAL node evaluates to low. In this case, a zero-gate delay occurs in the activation of switch MC2 (driving by the clock), whereas a 1.5-gate or more delay occurs in the pull-down of node EVAL. This

increases the pull-down time of node Y prior to its being pulled back up by action of the pull-up transistor MC3. (col. 2, lines 61-67) Glitching presents problems in several respects. For example, glitching raises power consumption and requires special care when conducting electromigration studies. Moreover, glitching reduces the noise margin for the circuit receiving the flop output. In addition, the problems of glitch propagation are intensified for low-voltage applications. FIG. 3(a) illustrates the case where Vdd=1.8v, and FIG. 3(b) illustrates the case where Vdd=1.0v. It is a common practice to attempt to counter glitching by skewing the inverter of the output buffer by selecting a stronger (lower beta ratio) pull-down device MN. When Vdd=1.8v as in FIG. 3(a), the voltage drive for MN is Vgs-Vt=0.9v-0.5v=0.4v in the case of a 50% glitch in the node Y potential. By using a larger MN in the inverter, some reduction in the glitch magnitude is possible. On the other hand, at the lower supply voltage Vdd=1.0v as in FIG. 3(b), the voltage drive for MN is Vgs-Vt=0.5v-0.5v=0.0v (again in the case of a 50% glitch in the node Y potential). Thus, regardless of the size of MN, the pull-down device is cutoff and can no longer hold the node down, and the glitch therefore propagates much more easily. There have been previous attempts to overcome or reduce the effects of glitching. One approach has been to speed up the discharge rate of the EVAL node by selecting large pull-down devices with low fanout for the EVAL node. This approach, while only minimally successful, increases the device area and power usage. Other designs include selecting a high beta ratio (i.e., a stronger pull-up) for MC3 relative to that of MC1 and MC2. Still other designs employ a high fanout on node Y by increasing the size of the output buffer INVB, or (as suggested above) a weakened pull-up (i.e. a small beta ratio) of the output buffer INVB to prevent propagation of the glitch. Nevertheless, any reduction in glitch magnitude is minimal with these approaches. (col. 3, lines 1-34)

Thus, *Tam* merely discloses how to avoid a glitch in a static flop circuit. Nothing in *Tam* shows, teaches or suggests a) a glitch error caused in a predetermined wire by an aggressor comprising one or more wires or b) replacing a driving circuit for driving a predetermined wire with another driving circuit having a

higher driving ability as claimed in claim 20. Rather, *Tam* is merely directed to avoiding or minimizing glitching in a static flop circuit.

D. Why the references taken as a whole do not suggest the claimed invention and why the features disclosed in one reference may not be properly combined with features disclosed in another reference

As discussed above, *Young et al* merely discloses inserting buffer circuits into a wire which would increase the number of elements in the circuit. Nothing in *Young et al* shows, teaches or suggests replacing a driving circuit with a driving circuit having a higher driving ability as claimed in claim 20.

Tam, as discussed above, is merely directed to minimizing glitch in the static output of a staticized flop circuit. Nothing in *Tam* shows, teaches or suggests determining a glitch error caused in a predetermined wire by an aggressor comprised of one or more wires or replacing a driving circuit with a circuit having a higher driving ability as claimed in claim 20.

A combination of *Young et al* and *Tam* would not be possible since the two are directed to different inventions. In other words, nowhere in either reference is it shown, taught or suggested how reducing glitch in the static output of a staticized flop circuit such as *Tam* would be associated with insertion of buffer circuits as in *Young et al.*

Even assuming *arguendo* that *Young et al* and *Tam* could be combined, the combination would merely suggest to add additional circuits to the existing circuitry as taught by *Young et al* and that, if a staticized flop circuit is used, to control the glitch of that circuit as taught by *Tam*. Thus, nothing in the combination of *Young et al* and *Tam* shows, teaches or suggests replacing a driving circuit with another one having a higher driving ability as claimed in claim 20. Furthermore, applicant respectfully submits that nothing in the combination of *Young et al* and *Tam* would show, teach or suggest the other features as claimed in claim 21.

For all of the above stated reasons, applicant respectfully requests the Board reverses the Examiner's rejection of claims 20-21 under 35 U.S.C. §103.

IX. Conclusion

For all of the above-stated reasons, applicant respectfully requests the Honorable Board of Patent Appeals and Interferences reverses the Examiner's decision in this case, since applicant respectfully submits that the final rejection of claims 20-21 is in error. Therefore, applicant respectfully submits that claims 20-21 should be allowed.

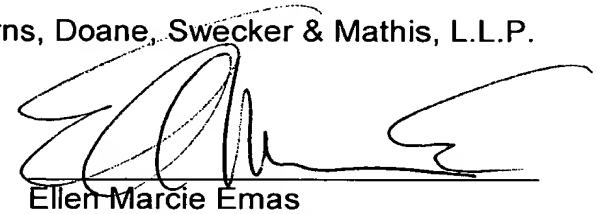
In the event that this paper is not timely filed within the currently set shortened statutory period, applicant respectfully petitions for an appropriate extension of time. The fees for such extension of time may be charged to our Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 02-4800.

Respectfully submitted,

Burns, Doane, Swecker & Mathis, L.L.P.

Date February 19, 2004

By: 

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APPENDIX A

The Appealed Claims

1. (Original) A circuit modification method of modifying a circuit by inserting one or more buffers into a predetermined wire located within the circuit, the method comprising the steps of:

determining whether a glitch error is caused in said predetermined wire by one or more aggressors each comprised of one or more other wires;

when determining that a glitch error is caused in said predetermined wire by one or more aggressors, determining one or more positions where one or more buffers are to be inserted into said predetermined wire based on a coupling capacity between each of said one or more aggressors and said predetermined wire.

2. (Previously Amended) A circuit modification method of modifying a circuit by inserting one or more buffers into a predetermined wire located within the circuit, the method comprising the steps of:

determining whether a glitch error is caused in said predetermined wire by one or more aggressors each comprised of one or more other wires;

when determining that a glitch error is caused in said predetermined wire by one or more aggressors, determining one or more positions where one or more buffers are to be inserted into said predetermined wire based on a coupling capacity between each of said one or more aggressors and said predetermined wire, wherein said insertion position determining step includes the steps of, when determining that a glitch error is caused in said predetermined wire by only one aggressor, calculating a target coupling capacity using the coupling capacity between said aggressor and said predetermined wire, and, when dividing said predetermined wire into a plurality of wire segments, determining one or more internal points of division of said predetermined wire so that a coupling capacity between each of said plurality of wire

segments and said aggressor does not exceed said target coupling capacity, and setting said one or more internal points of division to said one or more positions where said one or more buffers are to be inserted into said predetermined wire.

3. (Original) The circuit modification method according to Claim 2, wherein said target coupling capacity calculating step is the step of calculating said target coupling capacity by using an amount of glitch to be caused in said predetermined wire by said aggressor.

4. (Original) The circuit modification method according to Claim 3, wherein said target coupling capacity calculating step includes the steps of determining the number of said plurality of wire segments based on said amount of glitch, and calculating said target coupling capacity based on said coupling capacity between said aggressor and said predetermined wire and the number of said plurality determined in the above step.

5. (Original) The circuit modification method according to Claim 4, wherein said wire segment number determining step is the step of, when the coupling capacity between said aggressor and said predetermined wire is Cc, said amount of glitch is V, and a predetermined value is Vmax, determining the smallest integer number n which satisfies a following relationship: $V/n \leq Vmax$ as the number of said plurality of wire segments, and wherein said target coupling capacity calculating step is the step of calculating said target coupling capacity as follows: Cc/n, and said internal division point determining step is the step of determining said one or more internal points of division so that the coupling capacity between each of said plurality of wire segment and said aggressor is equal to said target coupling capacity Cc/n.

6. (Original) The circuit modification method according to Claim 3, wherein said target coupling capacity calculating step is the step of, when the coupling capacity between said aggressor and said predetermined wire is Cc, said amount of glitch is V, and a predetermined value is Vmax, calculating said target coupling capacity as follows: Cc*Vmax/V.

7. (Previously Amended) The circuit modification method according to Claim 2, wherein said one or more buffers to be inserted into said predetermined wire have a driving ability equal to or greater than that of a driving circuit for driving said predetermined wire.

8. (Original) The circuit modification method according to Claim 7, further comprising the step of selecting a type of buffer having a driving ability equal to or greater than that of said driving circuit for driving said predetermined wire and having a minimum area as each of said one or more buffers to be inserted into said predetermined wire from among a plurality of buffer cells stored in a cell library.

9. (Previously Amended) The circuit modification method according to Claim 2, further comprising the steps of, when determining that a glitch error is caused in said predetermined wire by one or more aggressors, replacing a driving circuit for driving said predetermined wire with another one having a higher driving ability than the driving circuit, and, before performing said insertion position determining step, determining whether a glitch error is caused in said predetermined wire driven by the other driving circuit by said one or more aggressors.

10. (Previously Amended) A circuit modification method of modifying a circuit by inserting one or more buffers into a predetermined wire located within the circuit, the method comprising the steps of:

determining whether a glitch error is caused in said predetermined wire by one or more aggressors each comprised of one or more other wires;

when determining that a glitch error is caused in said predetermined wire by one or more aggressors, determining one or more positions where one or more buffers are to be inserted into said predetermined wire based on a coupling capacity between each of said one or more aggressors and said predetermined wire, wherein said insertion position determining step includes the steps of, when determining that a glitch error is caused in said predetermined wire by a plurality of aggressors, calculating a plurality of target coupling capacities respectively associated with said plurality of aggressors by using the coupling capacity between each of said plurality of aggressors and said predetermined wire, and, when diving said predetermined wire into a plurality of wire segments, determining one or more internal points of division of said predetermined wire so that a coupling capacity between each of said plurality of wire segments and each of said plurality of aggressors does not exceed a corresponding one of said plurality of target coupling capacities, and setting said one or more internal points of division to said one or more positions where said one or more buffers are to be inserted into said predetermined wire.

11. (Original) The circuit modification method according to Claim 10, wherein said target coupling capacity calculating step includes the steps of, when the coupling capacity between each of said plurality of aggressors (referred to as *ith* (i=1 to k, k is the number of aggressors) aggressor hereafter) and said predetermined wire is Cc_i (i=1 to k), an amount of glitch to be caused in said predetermined wire by the *ith* aggressor is V_i (i=1 to k), and a predetermined value is Vmax, determining the smallest integer number n_i (i=1 to k) which satisfies a following relationship: $V_i/n_i \leq Vmax$ (i=1 to k) as the number of said plurality of wire segments for each of said plurality of aggressors, and calculating each of said plurality of target coupling capacities as follows: Cc_i/n_i (i=1 to k).

12. (Original) The circuit modification method according to Claim 10, wherein said insertion position determining step includes the steps of when dividing said predetermined wire into a plurality of wire segments for each of said plurality of aggressors, determining said one or more internal points of division of said predetermined wire so that the coupling capacity between each of said plurality of wire segment and each of said plurality of aggressor is equal to said corresponding target coupling capacity, and selecting said one or more positions where one or more buffers to be inserted into said predetermined wire from among all internal points of division determined in the above step for said plurality of aggressors.

13. (Original) The circuit modification method according to Claim 11, wherein said insertion position determining step includes the steps of when dividing said predetermined wire into a plurality of wire segments for each of said plurality of aggressors, i.e., said *ith* aggressor, determining said one or more internal points of division of said predetermined wire so that the coupling capacity between each of said plurality of wire segment and said *ith* aggressor is equal to said corresponding target coupling capacity Cc_i/n_i (i=1 to k), and selecting said one or more positions where one or more buffers to be inserted into said predetermined wire from among all internal points of division determined in the above step for said plurality of aggressors.

14. (Original) The circuit modification method according to Claim 10, wherein said target coupling capacity calculating step includes the steps of, when the coupling capacity between each of said plurality of aggressors (referred to as *ith* (i=1 to k, k is the number of aggressors) aggressor hereafter) and said predetermined wire is Cc_i (i=1 to k), an amount of glitch to be caused in said predetermined wire by said *ith* aggressor is V_i (i=1 to k), and a predetermined value is Vmax, calculating each of said plurality of target coupling capacities as follows: Cc_i*Vmax/V_i (i=1 to k).

15. (Original) A circuit modification method of modifying a circuit by inserting one or more buffers into a predetermined wire located within the circuit, the method comprising the steps of:

determining whether a glitch error is caused in said predetermined wire by an aggressor comprised of one or more other wires;

when determining that a glitch error is caused in said predetermined wire by an aggressor, determining a number of buffers to be inserted into said predetermined wire based on an amount of glitch to be caused in said predetermined wire by said aggressor.

16. (Original) The circuit modification method according to Claim 15, wherein said buffer number determining step is the step of, when said amount of glitch is V and a predetermined value is Vmax, calculating the smallest integer number n which satisfies a following relationship: $V/n \leq Vmax$.

17. (Original) The circuit modification method according to Claim 15, wherein said one or more buffers to be inserted into said predetermined wire have a

driving ability equal to or greater than that of a driving circuit for driving said predetermined wire.

18. (Original) The circuit modification method according to Claim 17, further comprising the step of selecting a type of buffer having a driving ability equal to or greater than that of said driving circuit for driving said predetermined wire and having a minimum area as each of said one or more buffers to be inserted into said predetermined wire from among a plurality of buffer cells stored in a cell library.

19. (Original) The circuit modification method according to Claim 15, further comprising the steps of, when determining that a glitch error is caused in said predetermined wire by one aggressor, replacing a driving circuit for driving said predetermined wire with another one having a higher driving ability than the driving circuit, and, before performing said buffer number determining step, determining whether a glitch error is caused in said predetermined wire driven by the other driving circuit by said one aggressor.

20. (Original) A circuit modification method comprising the steps of:

determining whether a glitch error is caused in said predetermined wire by an aggressor comprised of one or more other wires;

when determining that a glitch error is caused in said predetermined wire by an aggressor, replacing a driving circuit for driving said predetermined wire with another one having a higher driving ability than the driving circuit.

21. (Previously Presented) The circuit modification method according to claim 20, wherein said another driving circuit has a same function as the driving circuit.

APPENDIX B

Figures 1 and 4-6

APPENDIX B

Figures 1 and 4-6

FIG.1(a)

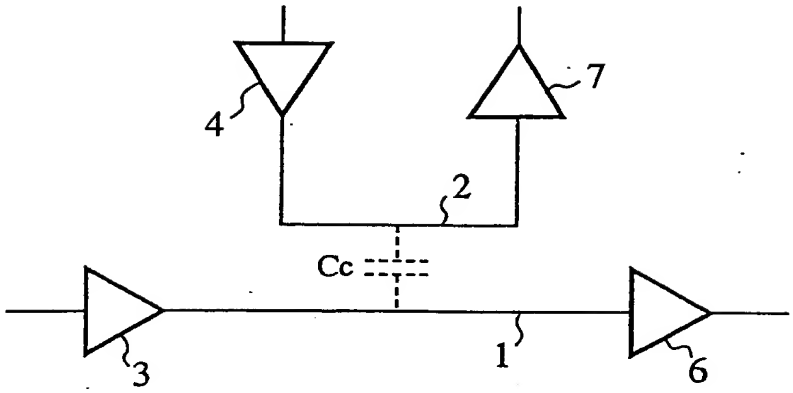

FIG.1(b)
(PRIOR ART)

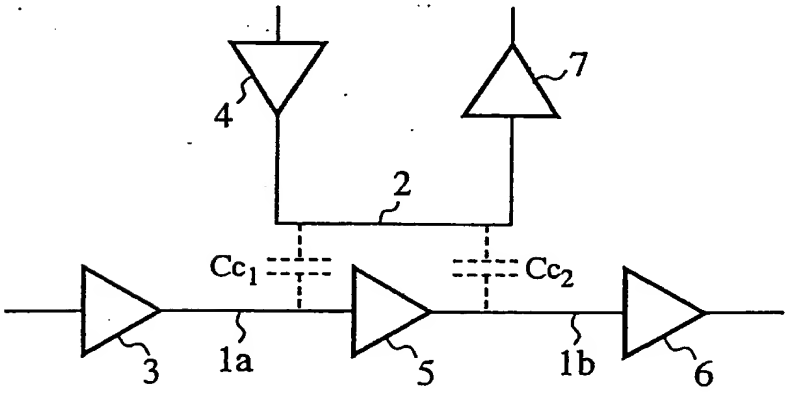

FIG.4(a)

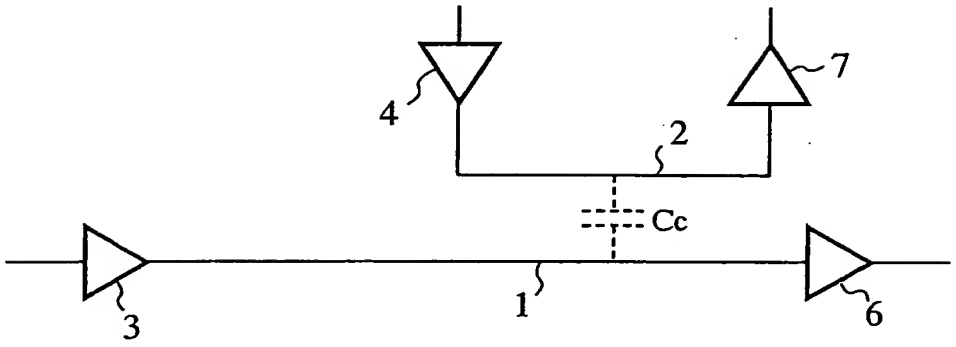

FIG.4(b)

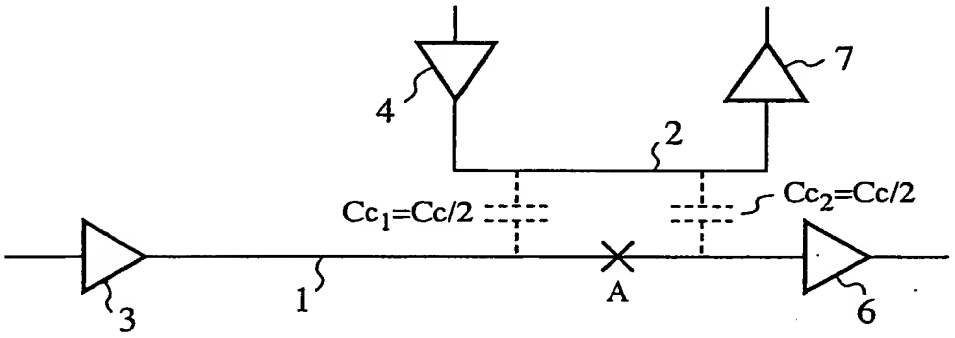

FIG.4(c)

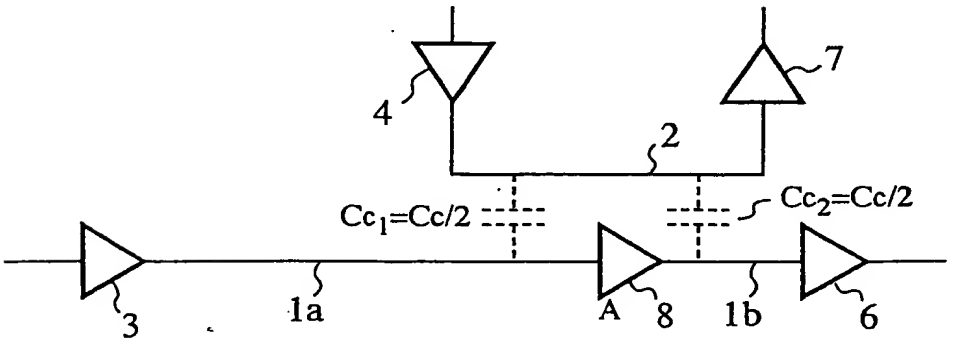

FIG.5(a)

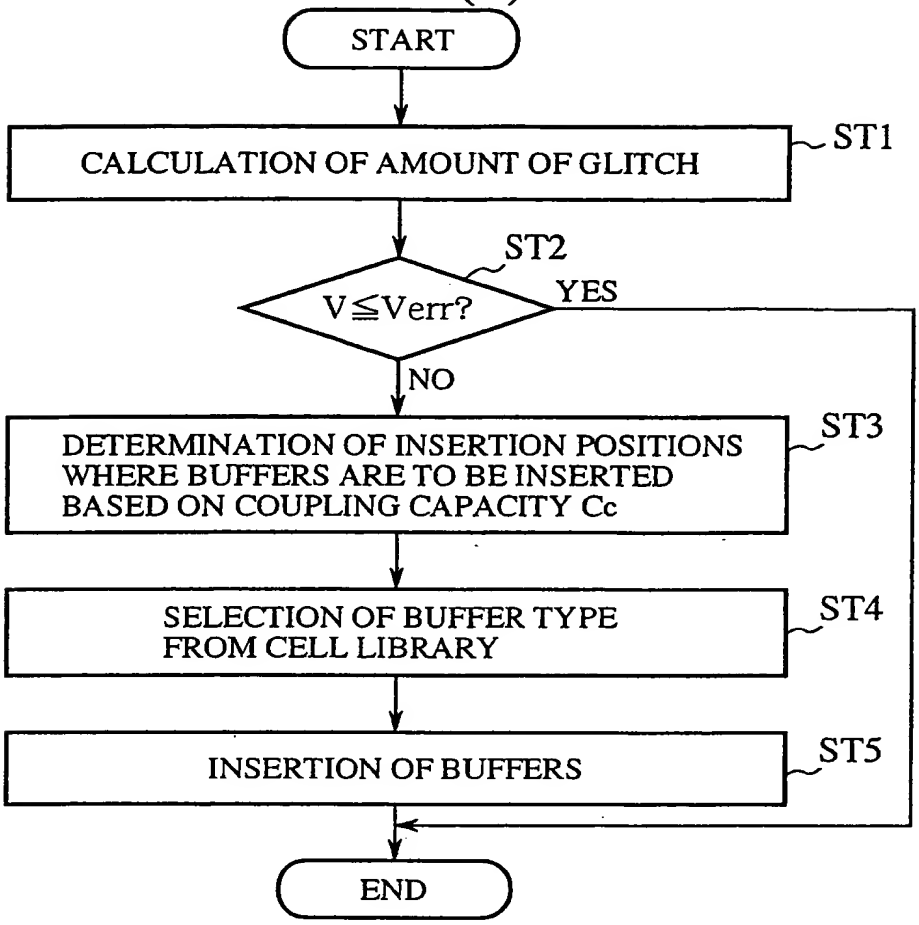

FIG.5(b)

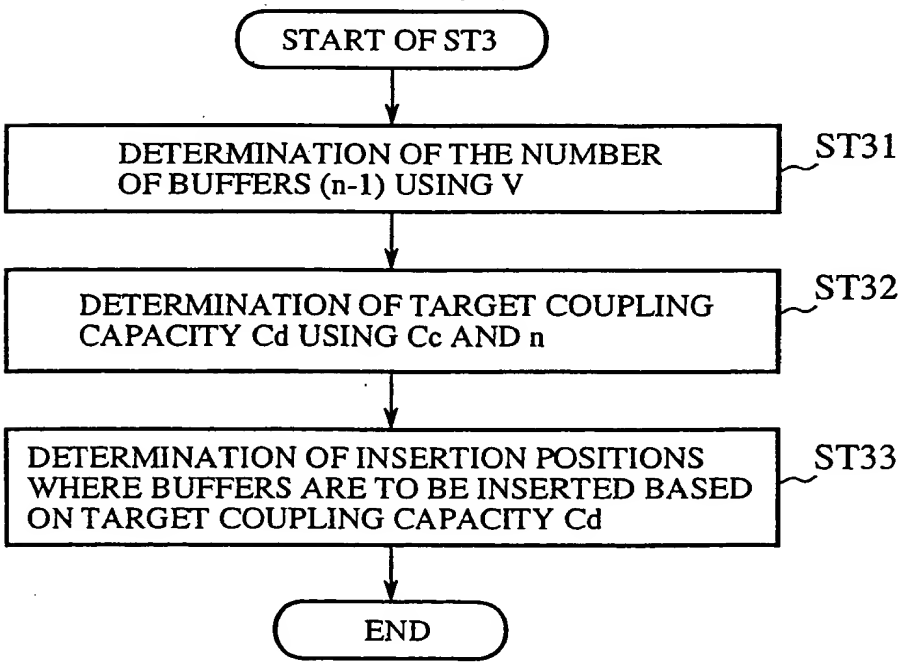

FIG.6

CELL TYPE	PARAMETERS			
	AREA	DRIVING ABILITY	. . .	. . .
INVERTER 1	X1(μm^2)	Y1(Ω)		
INVERTER 2	X2(μm^2)	Y2(Ω)		
DRIVER 1	X3(μm^2)	Y3(Ω)		
DRIVER 2	X4(μm^2)	Y4(Ω)		
NAND1	X5(μm^2)	Y5(Ω)		
NAND2	X6(μm^2)	Y6(Ω)		